a cross-functional team to satisfy the design for test (DFT) requirements on a challenging multi-die system-on-chip (SoC) project with a master die chiplet and four high-bandwidth memory (HBM) modules. We completed all DFT tasks and successfully shipped the product on schedule, at the target data rate, and without any impact on logic die size."

~Shinichiro Ikeda, Senior Principal Engineer, Socionext Inc.

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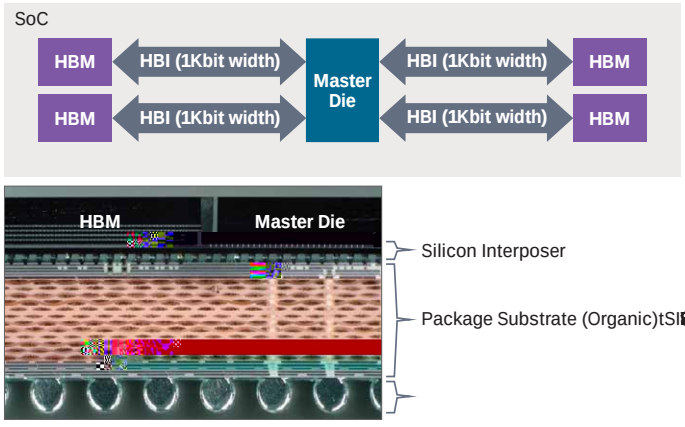
Challenges

Project Overview



design groups for Socionext and Synopsys

		Test Flow	Test Item	WT	FT	DA
	(a)	Master Die Test	Master Die Test (including other IPs)			–
			Master die logic scan test (including PHY IP)			–
SLM SHS IP	(b)	HBM PHY IP Test	Analog parts test (PLL and DLL test)			–
			At speed loop back test			–
	(c)	HBI Connection Test and Repair	HBI connection test and lane repair between SoC and HBM	–		–
SLM SMS ext-RAM IP	(d)	HBM DRAM Test	HBM test via DFT circuit in SoC	–		–
	(e)	HBM DA Test	Fault analysis by HBM vendor via DA port	–	–