SLM Clock & Delay Monitor IP

Measure delay between edges (Tcq, Tpd)

Highlights

- Accurate delay measurement between two edges
- No high-speed high accuracy reference clock required
- Low overhead for data processing
- Small form factor
- EDA integration for automated insertion and connection
- Capture state of silicon precisely at any stage of its lifecycle
- Accuracy is not affected by ageing

Use Cases

- Clock insertion delay
- Clock duty cycle
- Memory access time (Tcq)
- Delay line characteristic
- Ring oscillator frequency

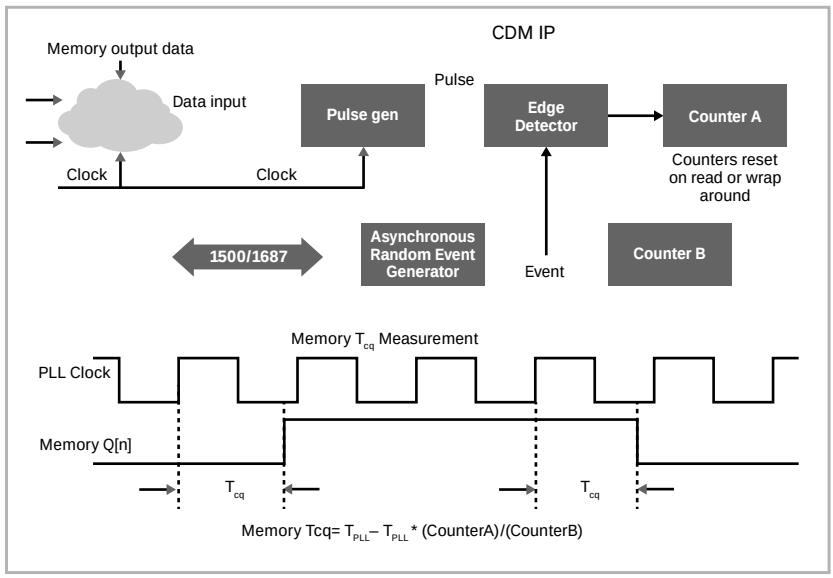

Figure 1: Synopsys SLM Clock & Delay Monitor IP

SLM Functional Monitors

Functional monitors are key to the success of Silicon Lifecycle Management (SLM). These monitors are embedded in the silicon and report out health of critical functions of the chip. Data from functional monitors can be collected at any stage of silicon lifecycle and analyzed to gather insights. Based on these insights actions can be taken to improve performance or mitigate an operational issue. Memory, CPU workload, interface, clock, delay, etc. are some critical functions on a SOC worth monitoring. Synopsys' functional monitors are enabled with EDA and software automation for ease of use.

Key Features

- No high-speed high accuracy reference clock required
- Small footprint
- Available as soft IP with flexibility to customize

Key Benefits

- Clock duty cycle quality check
- Memory access time tracking with BIST
- Digital delay line test characterization
- Optimize silicon performance for safety critical applications

Complete solution in SHS/SMS environment for Memory Read Time